ABSTRACT OF THE DISCLOSURE

A stack cache memory in a microprocessor and apparatus for performing fast speculative pop instructions is disclosed. The stack cache stores cache lines of data implicated by push instructions in a last-in-first-out fashion. An offset is maintained which specifies the location of the newest non-popped push data within the cache line stored in the top entry of the stack cache. The offset is updated when an instruction is encountered that updates the stack pointer register. When a pop instruction requests data, the stack cache speculatively provides data specified by the offset from the top entry to the pop instruction, before determining whether the pop instruction source address matches the address of the data provided. If the source address and the address of the data provided are subsequently determined to mismatch, then an exception is generated to provide the correct data.